

**COMPETITION SENSITIVE**

To: Distribution  
From: L. Facto, R. Graber, D. Gerke, J. Vasbinder

Subject: Magnitude-3 QA Survey and Engineering Evaluation, San Jose, CA, August 25-27, 1999

**Attendees:**

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**Purpose of Visit:**

JPL, LaRC, and GSFC conducted a preliminary evaluation at Magnitude-3 (M-3) in July 1998. At that time, M-3 (which was established 10/97) was in the process of setting up its assembly and test areas, as well as completing its converter designs. Due to M-3's stated focus on hybrid converters for space customers, and its extensive plans for optimizing circuit design and hybrid assembly, NASA personnel planned to monitor M-3's progress toward start of production lots and eventual QML certification.

Since that time, JPL has placed purchase orders with Magnitude-3 for flight hybrids for GRACE, GALEX, Mars'03, and MIRO projects. Due to hybrid delivery requirements of these projects, some of JPL's hybrid supplier evaluation tasks are being performed in parallel with M-3's assembly of flight lots. Three evaluation tasks were performed at M-3 on 8/25-27/99:

- QA survey
- Engineering evaluation of assembly and test capability
- Review of schematics and analysis reports

**Summary:**

Audit team findings are listed in Table 1. Action items for M-3 (Table 2) and JPL (Table 3) are included in this report. Significant topics are further detailed later in this report.

1. M-3's assembly processes and controls are generally good. A few (key) processes are still being optimized, but extra process monitors and/or interim processes are being utilized on current flight lots. There are a few ESD issues that must be resolved immediately. (M-3 is

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taking immediate action). JPL pre-seal visual and final inspections should be added to open P.O.s immediately.

2. M-3's test strategies, especially for electrical test and burn-in, are good. However, there is significant work that must be completed soon to avoid impacting schedules for GRACE and GALEX lots.
3. M-3's documentation of procedures is not as mature as JPL typically requires for flight lots. A traceability system for assembly is in place. M-3 will rely on a small group of experienced assemblers to build the flight lots. M-3's senior engineers will personally conduct all electrical and environmental testing. While this strategy should be successful on current JPL lots, it will be unacceptable for future lots if M-3 increases its staff without the necessary training and documentation in place.
4. Latest parts lists and radiation test reports are being reviewed by 514. Additional radiation testing will be performed by JPL 9/99 and by M-3 10/99. One hole in the data base will be low dose rate. If deemed necessary after parts list and data review, 514 will recommend piece part or hybrid low dose rate testing.
5. M-3 circuit designs for G and L series are generally good. Reports from 344 and 505 personnel are pending. Characterization testing by 344 is planned. Users will be notified of one application issue (involving use of inhibit function).
6. For G-series, worst case (WCA), stress, and thermal analysis reports are generally good. More detail for WCA will be provided to JPL. For L-series, stress and thermal analysis are generally good. JPL will review other L-series analysis as soon as it is available.

**Audit Notes:**

**I. Assembly: (see additional notes in Table 1)**

Line tours and document reviews were conducted 8/25-26/99. M-3's assembly areas include a clean room; an inventory, kitting and soldering room; and a laser trim room.

Assembly processes and controls were found to be generally good. It is important to note that the audit team bases this opinion mostly on observations during the line tour and on verbal answers given to our questions, rather than on good documentation of all assembly and inspection procedures. The risks associated with lack of mature documentation are mitigated only by the existence of a small group of 6 assemblers and 2 QA personnel who are (according to M-3 management) "highly experienced". This situation is believed to be tolerable for the current JPL flight lots. However, risk for future lots could be much greater if M-3's documentation and training is not fully in place before significant numbers of new assemblers are hired.

The general assembly sequence is:

1. Epoxy attach - low power semiconductors and small capacitors
2. High temperature solder reflow attach - power semiconductors

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3. Gold wire bond and non-destruct pull
4. Aluminum wire bond and non-destruct pull
5. Epoxy attach - magnetics
6. Low temperature solder reflow attach - power semiconductors, large capacitors, and most magnetic wires
7. Epoxy attach - substrate-to-package
8. Hand solder - package pins and small magnetic wires
9. Laser trim
10. Vacuum bake and seal

There are a few (significant) processes that M-3 is still optimizing, such as gold wire bonding and aluminum wire bonding.

Wire bonding:

For 1 mil gold wire bonding, M-3 recently stopped using a bonder from "manufacturer A" after this machine caused an extensive cratering problem on several chips. The first replacement bonder from "manufacturer B" exhibited an intermittent second bond problem. This machine is being repaired. The second replacement bonder from "manufacturer B" is producing good results on both first and second bonds. However, M-3 is not satisfied with the 2% occurrence of weak second bonds on this latest machine, and is continuing efforts to reduce the occurrence of these bonds.

All G and L series lots receive 100% non-destruct bond pull per M-3 data sheets. As an interim process monitor, M-3 is performing 100% destructive bond pull on 100 wires on a coupon substrate. Flight units are not bonded until acceptable coupon bond pull results are obtained. Acceptable results are all pulls  $\geq 2.5g$ , mean pull  $\geq 5g$ , and no bond lifts.

For 5 mil Aluminum wire bonding, M-3 has experienced weak substrate bonds after bake, in spite of normal pulls before bake. Bonding surfaces have been analyzed, with no contaminants found. Until M-3 determines the cause of the weak bonds, all aluminum bonds will be made to gold/nickel plated Kovar tabs mounted on the substrate, instead of directly to the substrate gold pads.

Sealing:

M-3 identified materials and cure schedules that would enable M-3 to meet RGA requirements, with the exception of the film capacitors. With the additional moisture outgassing from the film capacitors, a moisture getter is required to meet RGA requirements. M-3 has selected Alpha GA2000-02 PIND/moisture getter for flight lots. M-3's RGA results are ~500ppm moisture with this getter.

ESD:

Some observations from 7/98 were repeated during the latest visit, with a few new observations. Unacceptable or undesirable conditions include:

- computer monitor at work station near wire bonder and pull tester
- (a few) plastic containers on some work stations; no field meter used to check ESD safety
- metal table tops in the clean room instead of static dissipative
- units in work are transported in uncovered or partially covered metal "cookie trays" which use an upside down tray as lid

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- cloth wrist straps instead of metal

During the audit, M-3 was requested to immediately move the computer monitor, move the plastic items, and get a field meter, before flight lots reach these work stations. JPL volunteered to send a QA specialist to M-3 for an ESD audit and consultation on better ESD control procedures. JPL also volunteered to check its stock of containers for possible use by M-3.

Inspection of lots in work:

JPL inspected substrates in work for two GRACE lots. JPL commented on insufficient epoxy fillets on some ceramic capacitors, and appearance of non-wetting on some solder pads.

M-3 will correct the insufficient fillets immediately by adding epoxy by hand. Before more lots are processed, M-3 will review the epoxy screen process for proper epoxy thickness. M-3 stated that it must avoid too much epoxy, which will cause shorting. If the screen process cannot be optimized for small chips and large capacitors, then hand application of additional epoxy will be necessary on all future lots to achieve sufficient fillets on the larger capacitors.

The GRACE lots are being reworked to remove excess solder from the substrate pads before solder chip attach. Excess solder will cause the chips to be mounted with a tilt, which interferes with wire bonding. JPL commented that the uneven appearance of solder on the pads might be due to non-wetting in some areas, rather than to excessive solder in other areas. M-3 was requested to respond to this observation before the GRACE lots proceed further.

**II. Test: (see additional notes in Table 1)**

The test area includes electrical test, burn-in, and all screening except PIND and X-ray. PIND and X-ray will be performed at an outside lab.

Similar comments regarding lack of mature documentation for assembly procedures apply to test procedures. M-3 has a small staff of experienced design and process/test engineers that will personally conduct all hybrid screening. There are no test "operators" to train at this time.

Equipment: With the exception of burn-in boards, M-3 has procured all major test equipment required for hybrid screening and QCI testing. M-3's plans for test procedures and controls were found to be generally adequate. Although M-3's plans sound good, it should be noted that JPL's G and L series lots will be among the first (but not the very first) to use some of the fixtures, such as the burn-in boards and electrical test sockets.

Since all equipment is relatively new, and was delivered with calibration certifications from the equipment vendors, M-3 has not established a preventive maintenance and calibration control programs yet. Documentation for control procedures needs to be reviewed by JPL in the future.

Burn-in and life test: M-3 has received burn-in boards for G series and expects to receive boards for L series shortly. For both series, units are mounted to large heat sinks. LM35 temperature sensors are in contact with the heat sink under each hybrid. LM35 output and converter voltage output are continuously monitored. Over-temperature reading or faulty converter output readings will cause automatic removal of input power. There are also fuses on each converter input.

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Units are run with full load, 100% duty cycle, in an oven set to "a few degrees" below 125C, so that 125C case temperature is achieved. Little difference differences between hybrid case and oven air temperature is expected due to the large air flow in the oven. The oven's heater will shut down if the oven air temperature rises above the set point (planned to be 130 to 135C). Oven air flow and input power will continue to be supplied if the heater is shut down. (Continued air flow is good).

Electrical test: M-3 has received test sockets for G and L series. Test software is in work at M-3. Due to the absence of automated electrical test history, especially for the L-series, M-3 agrees to run a correlation unit at 3 temperatures before the post-burn-in electrical testing at 3 temperatures. JPL suggests that M-3 conduct 3 temperature testing at pre-burn-in on the first G and L-series lots, to provide an early warning of problems at temperature.

**III. Documentation (see additional notes in Table 1)**

Although the audit team believes that M-3's assembly and test procedures are generally good, the documentation of many of these procedures is incomplete. (JPL was aware of the general documentation status before the audit). Some documents are released, several documents are available as "preliminary", and some (especially in the test area) do not yet exist. The audit team reviewed several available documents, but obviously a follow-up visit to M-3 will be required when the documentation is more mature.

In lieu of a complete set of documented procedures and formal training for the assemblers, M-3 is relying on informal training of its small group of assemblers for current lots.

For hybrid testing, the engineers responsible for generating the test procedures will be personally conducting the testing on JPL's lots, since there are no other test operators at M-3 at this time.

Lot travelers do exist for the L and G series, and these were reviewed during the audit. Several minor comments are included in the action item list of Table 2. The most significant comment was the lack of requirements for JPL pre-seal visual and final inspections. JPL is in the process of correcting its P.O.s to add these requirements, but M-3 was requested to add these requirements immediately to the JPL travelers.

**IV Piece Parts**

Packages: For the G series, M-3 changed the package from AlSiC base and wall to AlSiC base and Kovar wall. This change was necessary due to hermeticity problems with the pin seals. The new package is approximately 8 grams heavier, so M-3 will revise its data sheet as necessary.

For the L series, the package is cold rolled steel with ceramic pin seals.

Substrates: For G series, one BeO substrate and two alumina substrates are used in each hybrid. All substrates are attached to the package with epoxy. The "A1" BeO input substrate has two configurations: 1 for 28V input, and 1 for 70V input models. The "A2" control substrate has two

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configurations: 1 for single and triple output, and one for dual output models. The "A3" output substrate has 3 configurations: 1 for single, 1 for dual, and 1 for triple output models. A3 substrates are populated differently for differently output voltage values.

For the L series, one alumina substrate is used in each hybrid. There are 3 configurations: 1 for 3.3V single, 1 for other singles, and 1 for duals.

Tantalum capacitors: Kemet type T495 are used. These are procured with current surge screening.

Film capacitors: These 2.2uF 100V capacitors are used instead of stacked ceramic capacitors. The capacitors are procured as a commercial product from Paktron, and upscreened at M-3 and an outside lab. M-3 provided its procurement documents, traveler, and supplier reliability information to JPL for review.

M-3 is still optimizing the pre-screening done on the film capacitors before these are installed in hybrids. A two step pre-screen is being performed at M-3 on capacitors for current JPL lots: 125V at 85C for 48 hours; plus 62.5V at 125C for 48 hours. These procedures might be modified on future lots, depending on screening yield at the hybrid level and results of planned capacitor life tests.

## **V. Radiation Hardness**

For the G series, M-3 provided a radiation test report on a 5V single model for JPL review. Testing was performed up to 2Mrads total dose and 90MeV-cm<sup>2</sup>/mg heavy ions. No low dose rate testing was performed.

For total dose, the G series 5V model may not be the worst case model, since it bypasses a portion of the feedback circuit that is used in other models. M-3 will perform total dose testing on 5V single, 12V dual, and 15V triple models at Sandia 10/99.

There has been one G series change since SEE testing was performed. A power MOSFET was changed from an SEGR rated type FSS230 to a 100k total dose rated type FRC230R. JPL will review the application derating of the new FET and assess the need for new SEE testing.

M-3 provided updated G and L series parts lists for JPL review. Previous reviews by JPL indicated a few concerns:

- Low dose rate: LM113 (lateral PNP) for G series
- (Low or High??) dose rate: 2N3501 for G and L series
- High dose rate: LS358 for G and L series

High dose rate issues should be resolved with available M-3 data and planned hybrid testing. M-3 is not planning any low dose rate testing. JPL will review the latest parts lists and determine whether low dose rate testing on piece parts or hybrids is recommended.

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Radiation test plans are:

G Series -

Total dose - by M-3 at Sandia 10/99 on one 5V single, and one 12V dual; 3 units to 300Krad minimum. These units will use current flight grade piece parts. Note that no TID testing on triple models is planned. Also, two to four of 5V duals will be tested with a new generation IR FET that is being evaluated for possible future use.

Neutron and dose rate - by M-3 at Sandia 10/99 on two 15V singles and one 15V triple. These samples will have FRC230R FETs. (Previous neutron samples had FSC230R FETs).

SEE - no additional testing planned by M-3

Also, LaRC is shipping 6 G series units to JPL for possible radiation (or other) testing; test plan and funding TBD.

L Series -

Total dose, dose rate, and neutron by M-3 at Sandia 10/99;

SEE - by JPL at Brookhaven 9/99 on 5V single

**VI. Schematic and Circuit Analysis Review**

Reviews were conducted by Vatche Vorperian and Tien Nguyen on 8/27/99, with Linda Facto also attending. Reports will be written by Vatche Vorperian for the schematic reviews, and by Tien Nguyen for the analysis reviews. I (L. Facto) do not believe any serious design problems were noted, but Vatche and Tien's documented assessments are needed.

For G series, all analysis (worst case, stress, thermal, FMEA, was available for Tien's review. For worst case analysis, he is awaiting more detailed schematic information for each section of the report before making final conclusions.

For L series, only the stress analysis and thermal analysis were available for review. Revision A of these reports is applicable to current JPL lots, which are rated for 40V input. Revision B of the reports is applicable to future lots after a change is made to one transistor from MSP650 to 2N3501. This change is necessary to achieve acceptable maximum junction temperature at 50V input, which is desired by some of M-3's customers.

For thermal analysis of G and L series, M-3 assumed 100% die attach coverage for epoxy attach elements and 70% attach for solder attach elements. M-3 explained that all power die are attached with solder. The largest die attached with epoxy is the PWM chip in L series, 128 X 96 mils. Within the next few months, M-3 plans to validate its thermal analysis by measuring junction temperatures of the larger chips in the hybrids.

JPL prefers that 50% coverage be assumed except where preforms are used. Depending on the outcome of M-3's junction temperature measurements, either M-3 or JPL should update the analysis with 50% attach coverage where appropriate.

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JPL needs to review the remaining L series analysis as it becomes available (by end 1999?)

Requests for additional information, and other action items related to these reviews, are included in Table 2.

**VII. DSCC Certification and Qualification Testing**

M-3's internal schedule for MIL-PRF-38534 certification from DSCC has slipped from "late 1999" (was once mid 1999) to mid 2000. This is primarily due to insufficient M-3 staff to generate all necessary documentation per earlier schedule predictions. M-3 plans to increase QA staff as soon as feasible to speed up documentation.

In lieu of DSCC certification, M-3 is performing Group C periodic inspection on the first flight lots for customers who do not waive Group C. This testing is being performed at M-3's cost for standard G and L series models. JPL is the first customer requiring full Group C.

Note that more rigorous Group C1 testing will be required for DSCC certification testing. Compared to periodic Group C testing, extra testing for certification includes 100 temperature cycles instead of 20, constant acceleration at 5000g instead of 3000g, and mechanical shock in addition to constant acceleration.



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Table 1. Summary of Audit Findings

I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
1	Substrate fabrication: BeO and alumina; up to 12 print layers; front and backside metal layers; 3 dielectric layers fired separately; solder pads are pure silver/ proprietary layer/Sn62; wire bond pads are gold; top glaze is "all or none" over printed resistors; can laser trim through glaze; use top glaze for G and L series	<ul style="list-style-type: none"> <li>• (OK for current P.O.s; want better doc on future lots)</li> <li>• Inspection docs not complete;</li> <li>• No acceptance docs other than traveler;</li> <li>• Need to add ink expiration dates to substrate traveler</li> </ul>	<ul style="list-style-type: none"> <li>• (Adequate with interim fix for Al wire bonding.)</li> <li>• Did not review in detail; processes established from former on-site company "Hybrid House"</li> <li>• No test on incoming ink lots; Rely on finished substrate test, including adhesion test, bondability test; visual</li> </ul>	<ul style="list-style-type: none"> <li>• (L) Al wire bonds on substrate are weak after hybrid screening; interim fix is to bond to tabs on substrate</li> <li>• (L) Mix inks from different vendors, but any problem should be evident after firing</li> </ul>
2	Adhesive attach Common epoxies; screen printing used for low power die and small caps; preforms used for substrate; chips placed by machine; awaiting info on RTV used for film caps and mag wire; numerous cures on each unit	<ul style="list-style-type: none"> <li>• OK</li> <li>• Record epoxy and RTV expiration dates on traveler</li> </ul>	<ul style="list-style-type: none"> <li>• (No; requested better fillets on larger caps; otherwise OK)</li> <li>• JPL lots in work have insufficient fillets on capacitors; need to add epoxy by hand until screen process optimized</li> <li>• Database for limited shelf life materials checked weekly and expired materials purged from assembly and stock areas</li> </ul>	<ul style="list-style-type: none"> <li>• (M) Check cap fillets at CSI precap; rework as needed; need to improve fillets on future lots</li> </ul>
3	Reflow solder chip attach On Sikama belt reflow with temperature ramp up/down and extra ceramic blank as buffer; done after epoxy chip attach; PbIn preforms for high temp solder of power chips before wire bond; Sn62 paste for large caps (Tantalum and some ceramic) after	<ul style="list-style-type: none"> <li>• OK</li> </ul>	<ul style="list-style-type: none"> <li>• (No; Need to address non-wetting issue on pads)</li> <li>• Filling space under film caps with RTV to stop solder ball shorts</li> <li>• Solder operations are outside clean room; Ensolve degreaser used afterward</li> <li>• New X-ray; will use in future for</li> </ul>	<ul style="list-style-type: none"> <li>• (M) Lots in work show non- wetting on substrate pads</li> <li>• (L) Power chips have gold or silver (both over nickel) backside; gold generally not desirable for PbIn attach, but M- 3 has had good results</li> <li>• (L) Still optimizing PbIn solder</li> </ul>

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I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
	wire bond; some power chips eutectically attached to moly tabs before tabs are attached to substrate.		process eval	process to eliminate tilted chips
4	Hand solder: Minimized; used only for 36 AWG wire and package pins; RMA flux	<ul style="list-style-type: none"> <li>• (Can tolerate for current P.O.s)</li> <li>• Special tools not called out on traveler</li> <li>• Solder iron temp control and grounding reqs not in process doc</li> </ul>	<ul style="list-style-type: none"> <li>•</li> </ul>	<ul style="list-style-type: none"> <li>•</li> </ul>
5 a	Gold wire bond: 1 mil; gold substrate pads; UVO pre-clean; recently stopped using "Manu. A" due to cratering problem; switched to "Manu. B"; same set-up for all gold bonds except rework	<ul style="list-style-type: none"> <li>• (Can tolerate for current P.O.s)</li> <li>• Need doc for K&amp;S bonder</li> <li>• UVO done "immediately prior" in practice, but doc does not have time limit between UVO and bonding</li> <li>• Need to decide on "in-line" or "end of line" Group B destructive bake/wire pull</li> </ul>	<ul style="list-style-type: none"> <li>• No; but can tolerate with extra interim bond pull</li> <li>• (interim) 100% destruct bond pull on coupon before</li> <li>• 100% nondestruct bond pull on production units</li> <li>• no SPC yet</li> <li>• ball shear testing used for process development; will do again for latest bonder;</li> <li>• Uses die bond pad etch (with wires intact) to evaluate bonding process for mechanical overstress</li> </ul>	<ul style="list-style-type: none"> <li>• (M) New bonder; still optimizing second bond while flight lots in work</li> </ul>
5 b	Aluminum wire bond: 5 mil; gold substrate pads; same set-up for all Al bonds	<ul style="list-style-type: none"> <li>• Preliminary doc written</li> </ul>	<ul style="list-style-type: none"> <li>• No; but can tolerate with interim bonding to tabs on substrate</li> <li>• 100% nondestruct bond pull on production units</li> <li>• no SPC yet</li> </ul>	<ul style="list-style-type: none"> <li>• (M) Investigating cause of weak Al substrate bonds after hybrid screening; bond surfaces not contaminated; interim fix is bonding to Au/Ni plated Kovar</li> </ul>

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I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
				tabs on substrate
6	Seal: 48 hour 150C vacuum bake in sealer; Seam weld; 15% He; monitor moisture & gas flow; PIND/moisture getter Alpha GA2000-02	<ul style="list-style-type: none"> <li>• Getter size not defined yet</li> <li>• Getter steps missing from G series traveler</li> </ul>	<ul style="list-style-type: none"> <li>• OK</li> <li>• Fine leak check immediately after seal</li> <li>• New machine; preventive maintenance schedule not established</li> </ul>	<ul style="list-style-type: none"> <li>• (L) Check JPL experience with selected getter</li> <li>• (L) Need preventative maintenance established for future</li> </ul>
7	Cleanliness and handling: Smocks, facemasks, hair nets, finger cots used; new filters for laminar hoods; very little clutter in work areas; use open metal tray with upside tray as lid for units in work	<ul style="list-style-type: none"> <li>• Must complete document set for all processes</li> </ul>	<ul style="list-style-type: none"> <li>• (Can tolerate for current P.O.s)</li> <li>• Need enclosed containers for mechanical, particle, and ESD protection</li> </ul>	<ul style="list-style-type: none"> <li>• (L) Soldering, laser trim outside clean room; rely on degreaser</li> <li>• (H) Stacked "Cookie trays" used - unprotected substrates or open packages can slide into each other if tray tipped</li> </ul>
8	ESD control: - Metal bench tops in clean room; static dissipative tops in solder and kitting areas; cloth wrist straps; metal trays for units in work	<ul style="list-style-type: none"> <li>• No</li> <li>• Need to require static dissipative work bench tops, document methods for daily and periodic verification and operation</li> </ul>	<ul style="list-style-type: none"> <li>• <b>No; need immediate action:</b> (a) move computer monitor away from wire bond/bond pull bench</li> <li>• (b) eliminate plastic containers from benches</li> <li>• (c) obtain field meter and use it</li> </ul>	<ul style="list-style-type: none"> <li>• (H) computer monitor on bench between wire bonder and pull tester</li> <li>• (M) metal bench tops can result in rapid discharge to units</li> <li>• (M) (a few) plastic items on bench tops; no field meter available to check danger</li> <li>• (M) Units transported in open metal trays with upside tray partially covering units</li> </ul>

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9	Electrical test: HP modules; will store all data; can use for trend tracking;	<ul style="list-style-type: none"> <li>Not available yet</li> </ul>	<ul style="list-style-type: none"> <li>OK for current P.O.s</li> <li>correlation units not established yet; will do 3 temp measurements on correlation unit after burn-in</li> </ul>	<ul style="list-style-type: none"> <li>(L) Test sockets for L and G series not checked out yet</li> <li>(L) Test software not finished yet</li> <li>(M) No FMEA on HP modules and power supply</li> <li>(L) No test docs yet; senior engineer to perform all set-up &amp; testing (risk will increase as test operators are hired, if doc not in place)</li> </ul>
10	Burn-in and life test: Full load 100% duty cycle at 125C; large heat sinks; oven has "high capacity" air flow	<ul style="list-style-type: none"> <li>Not available yet</li> </ul>	<ul style="list-style-type: none"> <li>Good control plans</li> <li>LM35 on heat sink is continuous temp monitor; input power shuts down for LM35 overtemp or failed converter output voltage;</li> <li>oven has overtemp shutdown for heater with continued air flow;</li> <li>5A fuses on converter inputs</li> </ul>	<ul style="list-style-type: none"> <li>(M) Need VIN &lt;=40V on current L series lots, due to use of MSP650 BJT without moly tab</li> <li>(L) L series boards not received yet</li> <li>(L) Test software not finished yet</li> <li>(L) No test docs yet; senior engineer to perform all set-up &amp; monitoring (risk will increase as test operators are hired, if doc not in place)</li> <li>(L) Oven profile done with unpowered, fully populated thermal load and with powered, half populated load (not with</li> </ul>

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I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
				fully populated powered load)
1 1	Other screening: Done at M-3 except X-ray and PIND done outside.	<ul style="list-style-type: none"> <li>Not available yet</li> </ul>	<ul style="list-style-type: none"> <li>Hot and cold temp monitor for temp cycling, but shutdown for hot over-temp only</li> <li>Will do FA on post burn-in failures</li> <li>Will notify JPL of post burn-in failures</li> </ul>	<ul style="list-style-type: none"> <li>(M) Most screening docs not done; using 883 test methods, senior engineers to perform all set-up and testing (risk will increase as test operators are hired, if doc not in place)</li> </ul>
1 2	<ul style="list-style-type: none"> <li>Training:</li> <li>ESD training done by QA Dir.;</li> <li>Assembly process training done by 2 assembly supervisors</li> </ul>	<ul style="list-style-type: none"> <li>Official training records not available until process docs released</li> </ul>	<ul style="list-style-type: none"> <li>On the job training adequate; small staff trained by supervisors</li> </ul>	<ul style="list-style-type: none"> <li>(L) No training records for review; relying on small, skilled staff of assemblers (risk will increase as operators are hired, if good training procedures not in place)</li> </ul>
1 3	QA/QC Involvement	<ul style="list-style-type: none"> <li>Many inspection and other QA docs not complete; will use 883 for final pre-seal visual</li> </ul>	<ul style="list-style-type: none"> <li>Direct observation by QA VP in lieu of finished docs</li> <li>Will use 883 for final pre-seal visual, which is not detailed enough for some hybrid processes</li> </ul>	<ul style="list-style-type: none"> <li>(L) relying on small, skilled staff of assemblers rather than QA oversight (risk will increase as operators are hired)</li> </ul>
1 4	CSI: Current JPL travelers state "when applicable" for precap and final	JPL error - CSI reqs missing from JPL P.O.	<ul style="list-style-type: none"> <li></li> </ul>	<ul style="list-style-type: none"> <li>(H) Fix travelers and P.O. ASAP for precap and final CSI</li> </ul>

**COMPETITION SENSITIVE**  
Table 1. Summary of Audit Findings

I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
1 5	Piece part test and control: <ul style="list-style-type: none"> <li>Element eval done by chip vendor or third party;</li> <li>stored in nitrogen cabinets; segregated for acceptance</li> </ul>	<ul style="list-style-type: none"> <li>Piece part SCDs adequate; some are preliminary</li> </ul>	<ul style="list-style-type: none"> <li>OK</li> <li>Good tracking database</li> </ul>	<ul style="list-style-type: none"> <li>(L) If waive element eval, might get parts from lots downgraded after failing H or K - current JPL lots already checked - are OK</li> <li>(M) Film cap screening and element eval still being optimized</li> </ul>
1 6	Lot traceability: <ul style="list-style-type: none"> <li>Reverse traceability exceeds 38534 reqs;</li> <li>also have forward traceability</li> </ul>	<ul style="list-style-type: none"> <li></li> </ul>	<ul style="list-style-type: none"> <li>OK - exceeds reqs</li> </ul>	<ul style="list-style-type: none"> <li></li> </ul>
1 7	Tooling/equipment control	<ul style="list-style-type: none"> <li>Not available yet</li> <li>Special tools not called out on traveler or process docs</li> </ul>	<ul style="list-style-type: none"> <li>Calibration system not set up yet</li> </ul>	(L) New equipment; calibrated as received (risk will increase with time and use if cal system not in place)
1 8	Document change control	<ul style="list-style-type: none"> <li></li> </ul>	<ul style="list-style-type: none"> <li>Use "Powerway Desktop" software as the control manager</li> <li>QA VP coordinates the control system; no other document manager specified</li> </ul>	<ul style="list-style-type: none"> <li></li> </ul>
1 9	Resources (personnel, equipment, etc.) 2 - QA, 2-EE, 2 - Process Engr, 2 - Prod. supervisors, 6 - operators, 1 - drafter/trimmer	<ul style="list-style-type: none"> <li></li> </ul>	<ul style="list-style-type: none"> <li></li> </ul>	<ul style="list-style-type: none"> <li>(H) Small staff; any departures could seriously impact remaining development activities and flight deliveries</li> </ul>

**COMPETITION SENSITIVE**  
 Table 1. Summary of Audit Findings

I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
2 0	Qualification test <ul style="list-style-type: none"> <li>• No formal Group C yet; series of "mini process quals" done to optimize materials and processes</li> <li>• Random vib not required by 38534, but done on G series</li> <li>• Mech. Shock not planned until DSCC qual in 2000.</li> </ul>	<ul style="list-style-type: none"> <li>• No qual data yet</li> </ul>	<ul style="list-style-type: none"> <li>• No qual test plan yet</li> </ul>	<ul style="list-style-type: none"> <li>• (H) First formal Group C testing to be performed on first JPL flight lots</li> <li>• (M) Random vib to be performed on JPL '03 Rover L series lot</li> </ul>

**COMPETITION SENSITIVE**

Table 1. Summary of Audit Findings

I T E M	ASSEMBLY/TEST/DESIGN AREA COMMENTS	DOCUMENTS ADEQUATE?	PROCESS CONTROL ADEQUATE?	TECHNICAL RISKS and RISK RATING (L/M/H)
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I T E M	DESIGN	<ul style="list-style-type: none"> <li>DESIGN RULES OR TEST DATA ADEQUATE?</li> </ul>	<ul style="list-style-type: none"> <li>ANALYSIS DOCUMENTATION ADEQUATE?</li> </ul>	<ul style="list-style-type: none"> <li>TECHNICAL RISKS and RISK RATING (L/M/H)</li> </ul>
2 1	Circuit analysis <ul style="list-style-type: none"> <li>G series - WCA, SA, TA, FMEA, rad complete</li> <li>L series - SA, TA complete</li> </ul>	<ul style="list-style-type: none"> <li>Design rules OK except used 100% die attach coverage</li> <li>Need more electrical test data over temperature</li> </ul>	<ul style="list-style-type: none"> <li>(Awaiting trip reports from Vorperian and Nguyen)</li> <li>Need to review updated SA, TA for L series for change to eliminate hot BJT</li> <li>Need to update (at JPL?) TA for 50% die attach coverage</li> </ul>	<ul style="list-style-type: none"> <li>(L) Need to review remaining analysis when completed, especially L Series WCA</li> <li>(M) Need to update TA for 50% die attach coverage</li> </ul>
2 2	Radiation hardness assurance For G series, will test each group of piece parts at the hybrid level.  For L series, plan is TBD. If initial hybrid TID tests indicate only a few chips have low margin, then perhaps RLAT will be done on these chips only.	<ul style="list-style-type: none"> <li>Design rules OK;</li> <li>G series data given to JPL for review</li> <li>Need data on L series; designed for 25Krad and no SEE to 37MeV-cm2/mg</li> </ul>	<ul style="list-style-type: none"> <li></li> </ul>	<ul style="list-style-type: none"> <li>(M) Need TID on L series (M-3 will test hybrids 10/99)</li> <li>(M) Need SEE on L series (JPL will test hybrids 9/99)</li> </ul>



Table 2. Action Items for M-3

Item No.	Description	M-3 Response	Status
<b>1 (HOT)</b>	Revise travelers for all JPL G and L series lots to add JPL pre-seal visual and final (pre-ship) inspection as requirements.	Travelers in production have been redlined and an ECO initiated to correct the master.	Closed 9/15/99
<b>2 (HOT)</b>	Add epoxy to ceramic capacitors, as needed, to JPL L series lots in work, to ensure proper filleting. Review epoxy screen printing set-up to improve fillets on future lots, or plan to add epoxy by hand after screen printing.	Epoxy has been added to production devices.  Do not have status on screen changes to improve fillet.	
<b>3 (HOT)</b>	Respond to JPL's concern regarding appearance of non-wetting or de-wetting on solder pads on current JPL L series lots.	Response with photos and data was supplied to JPL on 9/10/99. Results looked good.	Closed 9/15/99
<b>4 (HOT)</b>	Move computer monitor from vicinity of wire bond and wire pull stations to eliminate ESD issue.	Monitor was checked with a field meter by Rich Perry and also by Kirk Olsen from JPL. The monitor was determined not to be an ESD problem.	Closed 9/15/99
<b>5 (HOT)</b>	Eliminate plastic containers from workstations, and obtain field meter to check workstations.	Plastic containers will be removed. Plastic bottles for solvents was found not to be a problem, and confirmed by Kirk. We rented a field meter for two weeks to check out station. We are making corrections where needed.	Closed 9/15/99
<b>6 (HOT)</b>	Ensure that burn-in for current JPL L series lots is performed with <= 40V input voltage	Ed is working on it.	
<b>7 (HOT)</b>	Determine Group B test strategy (in line vs. end of line) for current lots.	Solderability will be done on a package from the same package lot. Internal Visual and Mechanical will be done at Pre-cap inspection. Physical dimensions and resistance to solvents will be performed at Final Inspection. Bond strength and die shear will be performed as part of Group C (subgroup 4). Seal test is 100% inspected after Final Test and prior to Final Inspection. A traveler will be initiated to capture traceability information.	
<b>8</b>	Finalize getter size, process for lots in work.	Harry is working on it.	

Table 2. Action Items for M-3

Item No.	Description	M-3 Response	Status
<b>(HOT)</b>			
<b>9 (HOT)</b>	Obtain sealable trays/containers that provide mechanical and ESD protection for substrates and packages in work.	Greg Christian from C.C. Steven came in at Kirk Olsen's request. We discussed with him what we needed and provided him with package samples. He is working with his suppliers to provide us with some solution options.	
10	Provide material and supplier name for these items, which are on the L series traveler, but are missing from the L series BOM: 172K-0008, 175K-0001, 175K-0002, 174K-0001, 961K-0004, 961K-0005. Correct the BOM.	This was provided to Linda Facto on 9/2/99.	Closed 9/15/99
11	L series traveler: Add material expiration dates for steps 6 and 41. Add tab PN for step 5. Add pre-form PN for step 8. Delete reference to "first BI" at step 63.	Travelers in production have been redlined and an ECO initiated to correct the master.	
12	Explain where tab and preform lot numbers are recorded for each assembly lot.		
13	G series travelers: Add getter steps. Add material expiration dates for step 6 of A1. Add tab PN for step 5 of A1. Add pre-form PN for step 1 of A3. Add to BOM: 172-0008, 174-0001, 175K-0001		
14	Provide copy of 251X-0003 for JPL review	These drawings have never been released and were/are in the process of being corrected/revised. SCDs 251x-0001 and 251x-0003 are largely irrelevant since Harris will not accept them or provide a C of C to them. Harris provides a C of C and data package for their MIL-PRF-19500 flow only. Therefore, the actual minimum requirements for these devices are defined in the purchase order. These drawings are currently being revised to reflect the device general characteristics, the receiving inspection requirements and the specific	

Table 2. Action Items for M-3

Item No.	Description	M-3 Response	Status
		requirements/instructions that are to be attached to each purchase order.	
15	Provide status of documents called out on G series traveler.		
16	Add ink expiration dates to substrate travelers.		
17	Obtain static dissipative workstation surfaces in assembly area (instead of metal).	We have requested quotations.	
18	Suggestion: Use metal ESD straps instead of cloth.	We have requested quotations.	
19	Revise wire bond documentation to cover new K & S bonders.		
20	Add special tool call-outs to travelers and/or process documents.		
21	Add solder iron temperature control and grounding requirements to process documents.		
22	Document interim process control procedures for gold wire bonding (100% destruct bond pull on coupon substrate).		
23	Document interim requirement for substrate tabs for Al wire bonds.	ECO in implementation adding tabs to all the assembly drawings.	
24	Report post burn-in yield to JPL on JPL lots. Perform FA on post burn-in electrical rejects.		
25	Run correlation unit at 3 temperatures prior to 3 temp post BI test on JPL lots.		
26	Suggestion: Perform 3 temp electrical test at pre burn-in on some or all of first JPL lots.		
27	251X-0002 for IRFC230 rev. NC - Why is FSS230 called out in 3.2.1.1.d? Why are element eval samples mounted with epoxy instead of solder?	SCD 251x-0002 was originally "cloned" from 251x-0001, which is the source control drawing for the FSS230R. It had been routed but languished for several weeks and was recently rejected for some of the issues later identified by JPL. It is in the process of being corrected for these issues as well as to properly identify both the non-radiation hardened and the radiation hardened versions of the IRF230 device.	
28	811X-0005 rev. A for CD5244B - Why is IR limit greater at -55C	Drawing has been corrected to reverse	

Table 2. Action Items for M-3

Item No.	Description	M-3 Response	Status
	than at 125C?	hot/cold subgroup identification?	
29	851X-0001 for MBR1645 rev. B - Why is VF limit higher at 125C than at -55C? Why do element eval samples call out 0.5 mil Al wire?	Drawing has been corrected to reverse hot/cold subgroup identification?	
30	Why are some docs rev NC, and others A, at initial release?		
31	Inform JPL of effectivity of change in L series Q1 from MSP650 to 2N3501 on moly. Inform JPL of change (if any) in burn-in input voltage related to this transistor change.		
32	Provide copies of Revision B of stress analysis and thermal analysis for L series.		
33	G series BOM: 451X-0002 is 54AC02 and BOM says 54AC04; 211X-0001 is 25V rated and BOM says 20V.		
34	Send loop analysis for L series to JPL. Include explanation of modeling method. Include measured data if available.		
35	Send input filter schematic for L series to JPL.		
36	Provide additional schematic information for each section of G series WCA report. Notify JPL when this information is available for review.		

Table 3. Action Items for JPL

Item No.	Description	Status
<b>1 (HOT)</b>	Revise P.O.s to include JPL QA pre-seal visual and final (pre-ship) inspections.	Repeated request 9/13 for this BPO change.
<b>2 (HOT)</b>	Provide further information to M-3 regarding ESD control procedures; send expert to M-3 for consultation.	Complete - JPL visit 9/14/99. See IOM DQA 99-254.
<b>3 (HOT)</b>	Check stock of containers for clean room areas that provide ESD and mechanical protection; send samples to M-3.	No appropriate JPL stock. Recommendations for container suppliers given to M-3 9/14/99.
4	Review latest parts list for reliability and radiation concerns and provide feedback to M-3.	Given to 514 rad group 9/10/99.
5	Review M-3 documentation for film capacitors and provide feedback.	Given to R. Herin 8/30/99.
6	Investigate getter GA2000-02.	Reviewed by E. Cuddihy & R. Graber - no negative comments.
7	Send M-3 available proton data for TL431A.	Request given to B. Rax.
8	Check for radiation concerns for film capacitors.	
9	Consider adding mechanical shock test to open P.O.s	
10	Inform users of degraded EMI performance for G and L series when inhibit pin is used.	
11	Pursue test plan and funding for G series units from LaRC (radiation or other?)	JPL SEE testing on 3 LaRC units done 9/16/99.